



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,357	07/18/2001	Louis J. Barbato	263/071	3265
34313 75	590 08/11/2005		EXAM	INER
ORRICK, HERRINGTON & SUTCLIFFE, LLP			CHAWAN, SHEELA C	
IP PROSECUTION DEPARTMENT 4 PARK PLAZA		ART UNIT	PAPER NUMBER	
SUITE 1600 IRVINE, CA 92614-2558			2625	
			DATE MAILED: 08/11/2005	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	09/909,357	BARBATO, LOUIS J.				
Office Action Summary	Examiner	Art Unit				
	Sheela C. Chawan	2625				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on 3.						
	action is non-final.					
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>28-46</u> is/are pending in the application.						
4a) Of the above claim(s) <u>1-27</u> is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>28-46</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or	r election requirement.	·				
Application Papers						
9) The specification is objected to by the Examiner.						
10) ☐ The drawing(s) filed on 18 July 2001 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a) All b) Some * c) None of:						
1. Certified copies of the priority documents have been received.						
 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage 						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413) 2) Notice of Draftsperson's Patent Drawing/Review (PTO-948) Paper No(s)/Mail Date						
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/10/03, 7/16/01.		Patent Application (PTO-152)				

Art Unit: 2625

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on October 25, 2004 has been entered and made of record.

Claims 1-27 are cancelled.

Claims 28-46 are pending in the application.

Election/Restriction

- 2. Claims 1-27 are withdrawn from further consideration pursuant to 37 CFR
- 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made without traverse filed on Oct 25, 2004.

Applicant's election without traverse, claims 28-46 Species II filed on Oct 25, 2004, is acknowledged.

Drawings

3. The Examiner has approved drawings filed on 7/18/01.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 4/10/03, the examiner has considered 7/18/01.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

Art Unit: 2625

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 28 - 30, are rejected under 35 U.S.C. 102(b) as being anticipated by Kannegundla et al., (US. 5,523,788) Listed in IDS date 4/10/03.

As to claim 28, Kannegundla discloses an electronics interface for interfacing to a multiplexed photo array comprising (fig 1, item 10 correspond to sensor) at Least one channel output (fig 1, item 12 ASP, corresponds to analog signal processing, column 3, lines 27-36), each one of the channel outputs capable of outputting a signal from each one of a plurality of photo detectors, each one of the plurality of photo detectors corresponding to a different image depth (column 3, lines 27-36), the electronics interface comprising:

at least one channel processor, each one of the channel processors (column 3, lines 18-21) having an input coupled to one of the channel outputs of the multiplexed photo array and an output, wherein each one of the channel processors acquires digital data from the respective channel output (column 3, lines 27-57);

a data bus (fig 1, item 28, coupled to the output of each one of the channel processors (note, output of ASP 12 reads on data bus); and

a memory buffer (fig 14 and 16) having an input coupled to the data bus and an output (note, input of memory buffer in fig 1, item 14 and 16 are connected to the output of ASP).

As to claim 29, Kannegundla discloses the electronics interface wherein the multiplexed photo array comprises exactly one channel output fig 1, item 10, column 3, lines 18-21).

As to claim 30, Kannegundla discloses the electronics interface of wherein the multiplexed photo array (fig 1, item 10) comprises exactly two channel outputs (fig 3, column 3, lines 21- 26, 54- 57).

Claim Rejections - 35 USC § 103

- 6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31- 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kannegundla et al., (US. 5,523,788) Listed in IDS filed on 4/10/03, as applied to the claims 28-30 above and further in view of Fujimoto (US.5, 588,434), Listed in IDS filed on 4/10/03.

Regarding claim 31, Kannegundla discloses a system architecture that utilizes digital signal processing circuitry designed to operate with single channel low resolution sensors to process the output data from high resolution dual channel image sensors.

Kannegundla is silent about the electronics interface comprising a digital-toanalog converter having an input coupled to the output of the memory buffer and an output.

Fujimoto discloses an ultrasonic diagnostic apparatus presenting closely correlated ultrasonic image. The system comprises of:

the electronics interface comprising a digital-to-analog (fig 1, 23) converter having an input coupled to the output of the memory buffer (fig 1, item 22, corresponds to video memory 22) and an output (fig 1, column 6, lines 7-15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Kannegundla to include a digital-to-analog converter having an input coupled to the output of the memory buffer and an output.

It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified Kannegundla by the teaching of Fujimoto in order to provide an ultrasonic diagnosing apparatus which offers a substantially less degraded image without the need for correction action by an operator even when the image is degraded due to the movement of a body to be diagnosed or of the transducer unit (as suggested by Fujimoto at column 2, lines 10- 15).

As to claim 32, Fujimoto discloses the electronics interface wherein the output of the digital-to-analog converter is coupled to an ultrasound console (fig 1, item 3, column 6, lines 7-15).

As to claim 33, Fujimoto discloses the electronics interface further comprising a

Art Unit: 2625

controller coupled (fig 1, item 2) to an ultrasound motor encoder (fig 1, item 74) for synchronizing the electronics interface and the multiplexed photo array with an ultrasound console column 6, lines 7-15).

As to claim 34, Fujimoto discloses the electronics interface the controller (fig 1, item 2, corresponds to ultrasonic control unit) instructs each one of the channel outputs of the multiplexed photo array (fig 1, item 4, plurality of transducer) to sequentially output the signal from each one of its respective plurality of photo detectors when the controller receives an encoder pulse from the ultrasound motor encoder (fig 1, item 74 corresponds to rotary encoder, column 7, lines 26-42).

As to claim 35, Fujimoto discloses the electronics interface wherein the controller (fig 1, 12) coordinates the timing of the channel outputs of the photo array and the channel processors such that each one of the channel processors acquires at least one digital datum for each photo detector signal outputted by the respective channel output (column 7, lines 26-42, column 22, lines 47-56).

As to claim 36, Fujimoto discloses the electronics interface wherein each one of the channel processors write its digital data into the memory buffer via the data bus (fig 1, column 6, lines 7-8).

As to claim 37, Fujimoto discloses the electronics interface, further comprising a digital-to-analog converter having an input coupled to the output of the memory buffer and an output coupled to the ultrasound console (fig 1, 23, column 6, lines 7 – 15, 41-67, column 7, lines 36-42).

Art Unit: 2625

As to claim 38, Fujimoto discloses the electronics interface, wherein the controller instructs the memory buffer to output the digital data received from the channel processors to the digital-to-analog converter when the controller receives a subsequent encoder pulse from the ultrasound motor encoder (column 16, lines 43-63, fig 1, fig 1).

As to claim 39, Fujimoto discloses the electronics interface, wherein the memory buffer (fig 1, 17, 18 and 19) outputs the digital data to the digital-to-analog converter in the form of a digital data Sequence (fig 1, 23).

As to claim 40, Fujimoto discloses the electronics interface, wherein the digital data in the digital data sequences (column 9, lines 3- 54) are arranged in order of increasing image depth (column 9, lines 3- 54, column 16, lines 59- 63).

As to claim 41, Fujimoto discloses the electronics interface, wherein the digital-to- analog converter the received digital data into an analog signal and outputs the analog signal to the ultrasound console (column 7, lines 36- 42, column 20, lines 53-65).

As to claim 42, Fujimoto discloses the electronics interface, wherein the digital-to-analog converter outputs the analog signal to the ultrasound console in the form of a serial analog signal (column 6, lines 7-15).

As to claim 43, Fujimoto discloses the electronics interface, further comprising a logic control (fig 1, 24) having an input coupled to the memory buffer and an output coupled to a digital input of the ultrasound console (column 6, lines 7-15).

As to claim 44, Fujimoto discloses the electronics interface, wherein the controller instructs the logic control to transfer the digital data stored in the memory

buffer to the ultrasound console when the controller receives a subsequent encoder pulse from the ultrasound motor encoder (column 5, lines 45- 62).

Page 8

As to claim 45, Fujimoto discloses the electronics interface, wherein the control logic transfers the digital data to the ultrasound console in form of a digital data sequence (column 5, lines 45- 62, column 6, line 54 through column 7, line 20).

As to claim 46, Fujimoto discloses the electronics interface, wherein the digital data in the digital data sequences are arranged in order of increasing image depth (column 5, lines 45- 62, column 6, line 54 through column 7, line 20, column 9, lines 3-54, column 16, lines 59- 63).

Other prior art cited

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cole et al., (US.6,363,033 B1) discloses method and apparatus for transmit beam former system.

Seppi et al., (US.5,692,507) discloses computer tomography apparatus using image intensifier detector.

Swanson (US.5,465,147) discloses method and apparatus for acquiring images using a CCD detector array and no transverse scanner.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheela C Chawan whose telephone number is. 571-272-7446. The examiner can normally be reached on Monday - Friday 7.30 - 4.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bhavesh Mehta can be reached on 571-272-7453. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheela Chawan

Patent Examiner

Group Art Unit 2625

August 5, 2005